

U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					M-12336 US		10/02/696	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)		Daniel C. Guterman et al.	
(Use several sheets if necessary)					Filing Date		October 31, 2001	
					Group		2817	

U.S. Patent Documents							
Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	4,173,766	11/6/79	Hayes			
	AB	4,527,257	7/2/85	Cricchi			
	AC	4,622,656	11/11/86	Kamiya et al.			
	AD	4,870,470	9/26/89	Bass, Jr. et al.			
	AE	5,043,940	8/27/91	Harari			
	AF	5,070,032	12/3/91	Yuan et al.			
	AG	5,095,344	3/10/92	Harari			
	AH	5,168,334	12/1/92	Mitchell et al.			
	AI	5,172,338	12/15/92	Mehrotra et al.			
	AJ	5,313,421	5/17/94	Guterman et al.			
	AK	5,315,541	5/24/94	Harari et al.			

Foreign Patent Documents							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL	EP 1 073 120 A2	1/31/01	Europe				
	AM	EP 1 091 418 A2	4/11/01	Europe				
	AN	EP 1 096 505 A1	5/2/01	Europe				
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
AQ	Eitan et al., "NROM: A novel localized trapping, 2-bit nonvolatile memory cell," <u>IEEE Electron Device Letters</u> , vol. 21, no. 11, November 2000, pp. 543-5.	
AR	Nozaki, "A 1-Mb EEPROM with a MONOS memory cell for a semi-conductor disk application," <u>IEEE Journal of Solid State Circuits</u> , vol. 26, no. 4, April 1991, p. 498.	
AS	Chan et al., "A true single-transistor oxide-nitride-oxide EEPROM device," <u>IEEE Electron Device Letters</u> , vol. EDL-8, no. 3, March 1987, pp. 93-95.	

Examiner	Date Considered
	1/15/03

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s)
(Use several sheets if necessary)		Daniel C. Guterman et al.
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October 31, 2001		281147

U.S. Patent Documents							Filing Date If Appropriate
*Examiner Initial	Document Number	Date	Name	Class	Subclass		
AA	5,343,063	8/30/94	Yuan et al.				
AB	5,426,605	6/20/95	Van Berkel et al.				
AC	5,436,481	7/25/95	Egawa et al.				
AD	B1 5,172,338	7/8/97	Mehrotra et al.				
AE	5,661,053	8/26/97	Yuan				
AF	5,712,180	1/27/98	Guterman et al.				
AG	5,768,192	6/16/98	Eitan				
AH	5,851,881	12/22/98	Lin et al.				
AI	6,011,725	1/4/00	Eitan				
AJ	6,030,871	2/29/00	Eitan				
AK	6,091,633	7/18/00	Cernea et al.				

	AK	6,091,633							
Foreign Patent Documents								Translation	
		Document	Date	Country	Class	Subclass	Yes	No	
	AL								
PTE (Including Author, Title, Date, Pertinent Pages, Etc.)									
PTE (Including Author, Title, Date, Pertinent Pages, Etc.)									

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AM	Eitan et al., "Hot-Electron Injection into the Oxide in n-channel MOS Devices," <u>IEEE Transactions on Electron Devices</u> , vol. Ed-28, no. 3, March 1981, pp. 328-340.
AN	D. Frohman-Bentchkowsky, <u>Applied Physics Letters</u> , Vol. 18, 1971, page. 332.
AO	D. Frohman-Bentchkowsky, "FAMOS - A new semiconductor charge storage device," <u>Solid-State Electron.</u> , 1974, vol. 17. P. 517
AP	Eitan et al., "Multilevel flash cells and their trade-offs," <u>IEDM Tech. Dig.</u> , 1996, pp. 169-172.
AQ	I. Fujiwara et al., "0.13 um MONOS single transistor memory cell with separated source lines," <u>IDEM Tech. Dig.</u> , 1998, pp. 995-998.

Examiner *[Signature]* Date Considered *10/16/03*

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U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.	Serial No.
					M-12336 US	10 02 696
INFORMATIONAL DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)					Applicant(s)	
					Daniel C. Guterman et al.	
					Filing Date	Group
					October 31, 2001	28184

U.S. Patent Documents							Filing Date If Appropriate
*Examiner Initial		Document Number	Date	Name	Class	Subclass	
AA	6.103.573	8/15/00	Harari et al.				RECEIVED JUL 24 2002 TECHNICAL CENTER 2800 JUL 25 2002
AB	6.104.072	8/15/00	Hirota				
AC	6.137.718	10/24/00	Reisinger				
AD	6.151.248	11/21/00	Harari et al.				
AE	US 6,201,282 B1	3/13/01	Eitan				
AF	US 6,215,148 B1	4/10/01	Eitan				
AG	US 6,222,762 B1	4/24/01	Guterman et al.				
AH	US 6,248,633 B1	6/19/01	Ogura, et al.				
AI							

Foreign Patent Documents							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AJ							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
AK	K. T. Chang et al., "A new SONOS memory using source-side injection for programming," <u>IEEE Electron Device Lett.</u> , vol. 19, 1998, pp. 253-255.
AL	P. J. Krick, "Three-state MNOS FET memory array," <u>IBM Technical Disclosure Bulletin</u> , vol. 18, no. 12, May 1976, pp. 1492-1493.
AM	Takashi HORI et al., "A MOSFET with Si-implanted Gate-SiO ₂ Insulator for Nonvolatile Memory Applications," <u>IEEE</u> , 0-7803-0817-4/92, pp. 17.7.1-17.7.4.
AN	D. J. DiMaria et al., "Electrically-alterable read-only-memory using Si-rich SiO ₂ injectors and a floating polycrystalline silicon storage layer," <u>J. Appl. Phys.</u> , 52(7), July 1981, pp. 4825-4842.
AO	"Basic Programming Mechanisms," <u>Nonvolatile Semiconductor Memory Technology - A Comprehensive Guide to Understanding and Using NVSM Devices</u> , IEEE Press series on microelectronic systems, 1998, pp. 9-25.
AP	Kamiya, M., et al., "EPROM Cell With High Gate Injection Efficiency," <u>International Electronic Devices Meeting of IEEE</u> , San Francisco, California, (Dec. 13-15, 1982) pps. 741-744

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U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Application No.
	M-12336 US	10/002,696
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicants	Confirmation No.
(Use several sheets if necessary)	Eliyahou Harari et al.	4652
	Filing Date	Art Unit Group
	October 31, 2001	2814

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
<i>[Signature]</i>	AA	4,398,248	Aug. 9, 1983	Hsia et al.			
<i>[Signature]</i>	AB	6,349,062	Feb. 19, 2002	Thurgate			
<i>[Signature]</i>	AC	6,366,501	Apr. 2, 2002	Thurgate et al.			
<i>[Signature]</i>	AD	6,406,960	Jun. 18, 2002	Hopper et al.			
	AE						
	AF						
	AG						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
<i>[Signature]</i>	AH	SU 960953 A	23 Sept. 1982	Soviet Union			Abstract	X
	AI							
	AJ							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>[Signature]</i>	AK	Chen, Wei-Ming et al., "A Novel Flash Memory Device with <u>S</u> plit Gate Source Side Injection and <u>O</u> NO Charge Storage Stack (SPIN)", 1997 Symposium on VLSI Technology Digest of Technical Papers, pp. 63-64.
<i>[Signature]</i>	AL	Roizin, Yakov, et al., "Novel Techniques for Data Retention and Leff Measurements in Two Bit <u>micro</u> FLASH [®] Memory Cells", AIP Conference Proceedings, Volume 550, Melville, New York, 2001, pp. 181-185.
<i>[Signature]</i>	AM	Hsia, Yukun, "Memory Applications of the MNOS", Wescon Technical Papers, Volume 16, 1972, pp. 3303-3308.

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AA		4,112,507	Sept. 5, 1978	White et al.				
AB		5,887,145	Mar. 23, 1999	Harari et al.				
AC		6,281,075	Aug. 28, 2001	Yuan et al.				
AD								
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AH								
AI								
AJ								
AK								
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
AM	Hayashi, Yutaka et al., "Twin MONOS Cell With Dual Control Gates", 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 122-123.							
AN								
AO								
Examiner			Date Considered					
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